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TRANSMITTAL FORM (to be used for all correspondence after initial filing)	Application Number	09/977,031	
	Filing Date	October 12, 2001	
	First Named Inventor	Stephen O'Connor	
	Group Art Unit	Unknown	
	Examiner Name	Unknown	
Total Number of Pages in This Submission	5	Attorney Docket Number	PA1971US

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SIGNATURE OF APPLICANT, ATTORNEY, OR AGENT	
Firm or Individual name	Carr & Ferrell, LLP Cust. No. 22830
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UNITED STATES PATENT AND TRADEMARK OFFICE

APPLICANT: Stephen O'Connor
SERIAL NO.: 09/977,031
FILED: October 12, 2001
TITLE: Multistage Pipeline Bit Conversion
EXAMINER: Unknown
GROUP ART UNIT: Unknown
ATTY.DKT.NO.: PA1971US

COMMISSIONER FOR PATENTS
WASHINGTON, D.C. 20231

INFORMATION DISCLOSURE STATEMENT Under 37 C.F.R. §§ 1.56, and 1.97-1.98

SIR:

Pursuant to the provisions of 37 C.F.R. §§ 1.56 and 1.97-98 of the Rules of Practice in Patent Cases, enclosed herewith is form PTO-SB-08 listing several references, copies of which are enclosed. The Examiner is requested to make these references of official record in the application. The references cited may be material to examination of the

application and are submitted in compliance with Applicant(s)'s duty of disclosure as defined by 37 C.F.R. § 1.56.

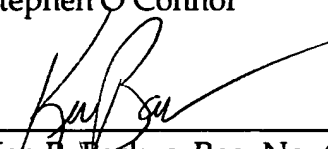
No representation is made or intended as to the completeness of this list, nor is the inclusion of any reference on this list an admission that it is prior art or pertinent to this application.

Respectfully submitted,

Stephen O'Connor

Dated: January 18, 2002

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Sheet 1 of 1

Compleat if Known

Application Number	09/977,031
Filing Date	October 12, 2001
First Named Inventor	Stephen O'Connor
Group Art Unit	Unknown
Examiner Name	Unknown
Attorney Docket Number	PA1971US

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		10 Gigabit Ethernet Alliance [online]. "10 Gigabit Ethernet Technology Overview White Paper", May, 2001 Revision 1.0. Retrieved from Internet: <URL: http://www.10gea.org >.	
		AGERE SYSTEMS, "10 Gigabit Ethernet PCS Intellectual Property Cores (Preliminary Data Sheet)", July 2001. Retrieved from <URL: www.agere.com >.	
		DUGAN, et al., "64b/66b Coding Update" [Presentation Materials], IEEE 802.3ae, Albuquerque, NM, March 6, 2000.	
		MCCARLEY [Initiator of discussion], 'Re: 64b/66b gearbox in FPGA.' (Threaded Discussion on the Comp.arch.fpga vsnet newsgroup) [online], Jan./Feb., 2001. Retrieved from Internet:<URL: www.fpga-faq.com/archives/28975.html > and similar pages [retrieved on 22 June 2001].	

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